Amendments to the Drawings:

The attached replacement drawing sheets make changes to Figs. 7 and 8 and replace the original sheets with Figs. 7 and 8.

Attachment: Replacement Sheets

REMARKS

Claims 10-12, 14, and 23 are pending in this application. By this Amendment, claim 10 and the drawings are amended. No new matter is added.

Applicant included claims amendments that were marked relative to the wrong version of the claims in the Response to Quayle Action filed on February 12, 2007. To remedy this error, the claim amendments presented in this Substitute Response are marked relative to the correct version of the claims, i.e., the claims entered by the November 20, 2006 Amendment After Final Rejection. Fig. 8 has also been amended in a slightly different manner than presented in the February 12, 2007 Response to Quayle Action based on the Examiner's suggestion in a March 8, 2007 telephone conversation. The Remarks presented in the February 12, 2007 Response to Quayle Action are duplicated below, with a minor modification based on the Examiner's suggestion regarding Fig. 8.

The Quayle Action objects to the drawings under 37 C.F.R. §1.83(a) for not showing "n(n≥2) gate-output pulses are supplied to the scanning driver at a different timing within one vertical period in a picture signal" and "the scanning driver shifts each of the n (n≥2) gate-output pulses in synchrony with the clock signals." Those of ordinary skill in the art would understand that at least Figs. 7 and 8 disclose the above-mentioned features. However, Figs. 7 and 8 have been amended to include captions to already existing and labeled features.

Fig. 7 is a timing chart that shows clock signal CLY, gate-output pulse DY, and vertical synchronization signal VSYNC for a case when n=2. The description of Fig. 7 notes that the Figure shows "a gate-output pulse DY being output twice during one vertical period" (i.e. when n=2). Further, the description of Fig. 7 notes that the gate-output pulse DY is supplied to the scanning driver.

Fig. 8 is a timing chart illustrating an enlargement of the symbol "A" in Fig. 7. Fig. 8 shows gate-output pulse DY, clock signal CLY, enable signal ENB 1, enable signal ENB 2

and scanning lines G_1 through G_{m+1}. The description of Fig. 8 notes that the gate pulse is sequentially output in a sequence, such as from G_1 through G_{m+1}. Thus, one of ordinary skill in the art would understand that the gate-output signals are shifted in synchrony with the clock signals when viewing the clock signals shown in Fig. 8, as well as, for example, the gate-output pulse shown on G_1 with respect to the gate-output pulse shown on G_{m+1}.

Since this application has been amended to address the formal issues raised in the Office Action, Applicant respectfully submits that this application is in condition for allowance.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

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JAO:AEG/jnm

Date: April 18, 2007

Attachment: Replacement Drawing Sheets

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FIG. 7